LQD400-ER4

QSFP-DD 400Gb/s ER4 40km DDM Transceiver

PRODUCT FEATURES

- Supports 400GBASE-ER4
- Lane bit rate 106.25Gb/s with PAM4
- Up to 40km transmission on SMF
- 400GAUI-8 Electrical interface with 8 Lanes
- 53.125 Gb/s PAM4 high-speed signal
- I2C interface with integrated Digital Diagnostic monitoring
- QSFP-DD MSA package with duplex LC connector
- Single +3.3V power supply
- Maximum power consumption 12W
- Operating case temperature: 0 to +70 °C
- Complies with EU Directive 2015/863/EU

APPLICATIONS

- 400GBASE-ER4 Ethernet (PAM4)
- 5G Back-haul / Data center / Cloud application

Ordering information

Part No.	Data Rate	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI
LQD400-ER4	425Gbps	EML	SMF	40km	LC	0~70 ºC	Y

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.5	-	+3.6	V	
Operating Relative Humidity	R_H	-	-	+85	%	

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	T_C	0	-	70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Power Dissipation	P	-	-	12	W	
Pre-FEC Bit Error Ratio	Pre-FEC BER	-	-	$2.4x10^{-4}$		1
Post-FEC Bit Error Ratio	Post-FEC BER	-	-	1×10^{-12}		1
Transmission Distance	TD	-	-	40	km	2

Notes:

1. FEC provided by host system.

2. FEC required on host system to support maximum distance.

III. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Signaling rate, each lane	BR	53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	L0	1304.06	1304.58	1305.1	nm	
	L1	1306.33	1306.85	1307.38	nm	
	L2	1308.61	1309.14	1309.66	nm	
	L3	1310.9	1311	1311.96	nm	
Total average launch power	P_{MAX}	-	-	10	dBm	
Average launch power, each lane	P_{OUT}	1.5	-	7.1	dBm	1,2
Outer OMA, each lane	OMA_{outer}	4.5	-	7.9	dBm	3
Difference in launch power between lanes		-	-	4	dB	
Transmitter and dispersion eye closure for PAM4	TDECQ	-	-	3.9	dBm	
Transmitter eye closure for PAM4 (TECQ),	TECQ	-	-	3.9	dBm	

each lane(max)						
|TDECQ – TECQ|		-	-	2.7	dB	
Average POUT (Laser Turn off)	P_{OFF}	-	-	-30	dBm	
Extinction ratio, each lane	ER	6	-	-	dB	
Side-mode suppression ratio	SMSR	30	-	-	dB	
Receiver						
Signaling rate, each lane	BR	53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	L0	1304.06	1304.58	1305.1	nm	
	L1	1306.33	1306.85	1307.38	nm	
	L2	1308.61	1309.14	1309.66	nm	
	L3	1310.9	1311	1311.96	nm	
Damage threshold, each lane	P_{DAMAGE}	-2.4	-	-	dBm	4
Average receive power, each lane	P_{RX_LANE}	-16.2	-	-3.4	dBm	5
Receive power (OMA_{outer}), each lane	RX_{OMA}	-	-	-2.6	dBm	
Receiver sensitivity (OMA_{outer}), each lane	SEN_{OMA}	-	-	-14	dBm	6
Los Assert	LosA	-30	-	-20	dBm	
Los De-assert	LosDA	-	-	-17	dBm	
Los Hystersis	LosH	0.5	-	-	dB	

Notes:

1. As the total average launch power limit has to be met, not all of the lanes can operate at the maximum average launch power ,each lane.
2. Average launch power, each lane(min) is informative and not the principal indicator of signal strength.A transmitter with launch power below this value cannot be compliant: however, a value above this does not ensure compliance.
3. Even if the TDECQ<1.4dB for an extinction ratio of >=4.5dB or TDECQ<1.3dB for an extinction ration of <4.5dB, the OMAouter (min) must exceed this value.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
5. Average receive power, each lane(min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Measured with conformance test signal at TP3 for the BER specified in 122.1.1 802.3cn-2019.

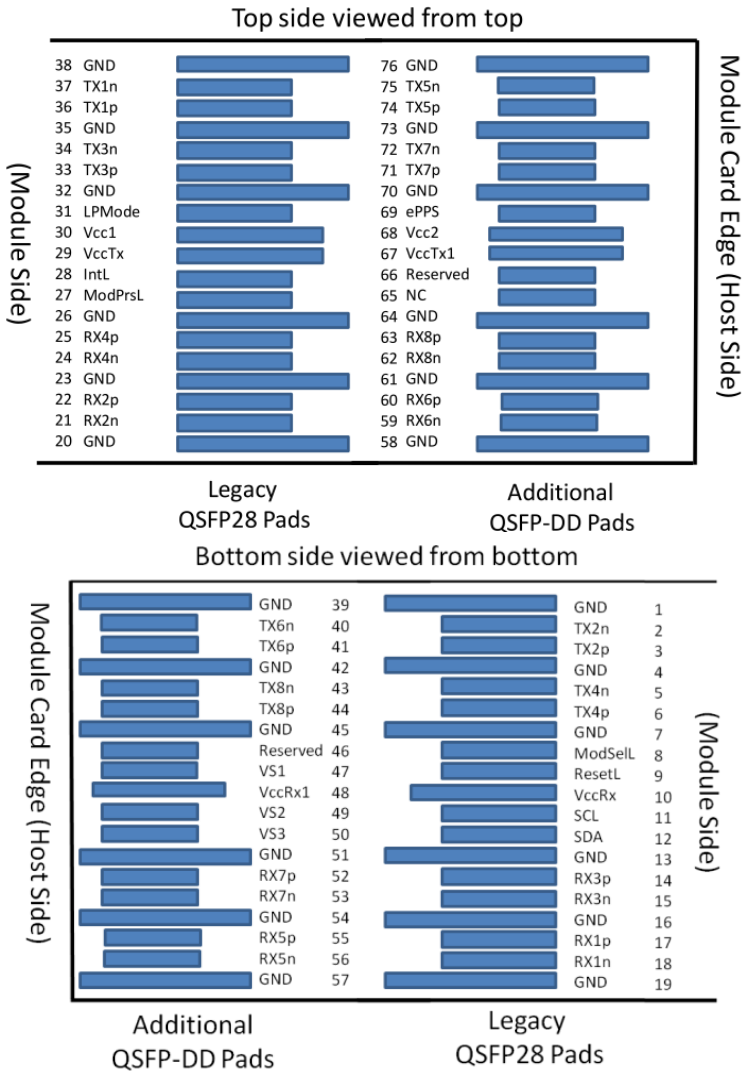
IV. Electrical Characteristics

Parameter		Symbol	Min.	Typical	Max.	Unit
Transmitter (Module Input)						
Differential Data Input Amplitude		$V_{IN,P-P}$	70	-	900	mVpp
Differential Termination Mismatch			-	-	10	%
Tx_Disable	Normal Operation	V_{IL}	-0.3	-	0.8	V
	Laser Disable	V_{IH}	2.0	-	V_{CC}+0.3	V
Receiver (Module Output)						
Differential Data Output Amplitude		$V_{OUT,P-P}$	200	-	900	mVpp
Differential Termination Mismatch（1MHZ）			-	-	10	%
Rx_LOS	Normal Operation	V_{OL}	-	-	0.4	V
	Lose Signal	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V

V. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current per lane	0 to 100	10%	mA	Internal
Tx Output Power per lane	1.5 to 7.1	±3	dBm	Internal
Rx Power per lane	-16.2 to 3.4	±3	dBm	Internal

VI. Pin Diagram



VII. Pin Descriptions

PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1B	1

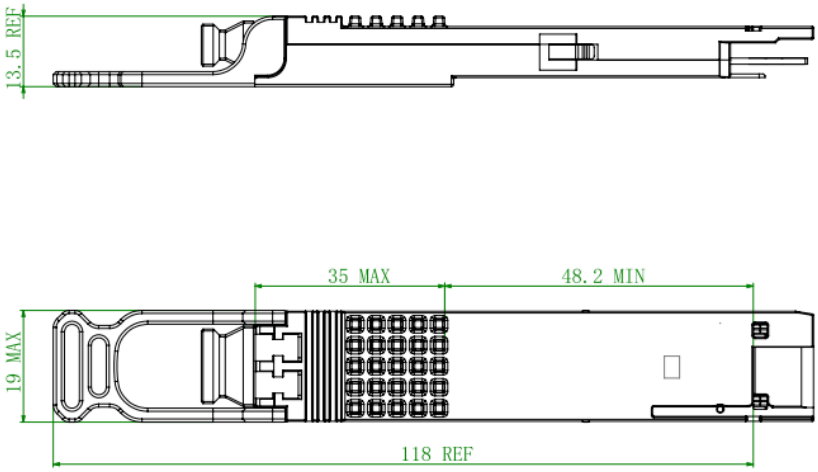
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTLL-I	ModSelL	Module Select	3B	
9	LVTLL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RX_LOS	Interrupt/Rx LOS	3B	
29		VccTx	+3.3 V Power Supply transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power mode/Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	

45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

VIII.Mechanical Specifications(Unit: mm)



Revision History

Version No.	Date	Description
1.0	June 16, 2021	Preliminary datasheet

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