

LQP40-DAC-xxx

QSFP+ Direct Attach Passive Copper Cables, 1m, 2m, 3m, 4m, 5m Reach

PRODUCT FEATURES

- Up to 40GBd bi-directional data links
- Compliant with QSFP+ MSA specifications
- Fully Compliant with IEEE802.3ba specifications
- 4 independent duplex channels operating at 10Gbps,also support for 2.5Gbps, 5Gbps data rates
- AC coupled inputs and outputs
- 100 Ohm differential impedance
- All-metal housing for superior EMI performance
- Single power supply 3.3V, low power consumption
- RoHS Compliance
- Operating temperature: 0°C to +70°C

APPLICATIONS

- Servers
- Networked storage systems
- Routers
- External storage systems
- Data Center networking



Product Description

QSFP+ (Quad Small Form-factor Pluggable Plus) Copper direct-attach cables are suitable for very short distances and offer a highly cost-effective way to establish a 40-Gigabit link between QSFP+ ports. QSFP+ are designed for a high-density cabling interconnect system capable of delivering an aggregate data bandwidth of 40Gbps. This interconnect system is fully compliant with QSFP+ MSA. The QSFP+ cables support the bandwidth transmission requirements as defined by IEEE802.3ba(40Gbps).

Ordering Information

Part Number	Description	Cable Length (m)	AWG	
LQP40-DAC-001	QSFP+ to QSFP+	1	30	
LQP40-DAC-002	QSFP+ to QSFP+	2	30	
LQP40-DAC-003	QSFP+ to QSFP+	3	30	
LQP40-DAC-004	QSFP+ to QSFP+	4	26	
LQP40-DAC-005	QSFP+ to QSFP+	5	26	

Note: You can be customized diameter and distance.

I. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input impedance	Zin	90	100	110	ohm	
Operating Case Temperature	Торс	0		70	degC	
Storage Temperature	Tst	-40		85	degC	
Relative Humidity (non- condensation)	Rs			85	%	
Supply Voltage	Vcc3	3.135		3.465	V	
Voltage on LVTTL Input	Vi lvttl	-0.3		Vcc3+0.2	V	

II. Mechanical Specifications

Parameter	Min	Typical	Мах	Unit
Cable Diameter (24 AWG)		0.385		Inches
Bend Radius (24 AWG)	1.929			Inches
Cable Diameter (26 AWG)		0.346		Inches
Bend Radius (26 AWG)	1.732			Inches
Cable Diameter (28 AWG)		0.295		Inches
Bend Radius (28 AWG)	1.476			Inches
Cable Diameter (30 AWG)		0.259		Inches
Bend Radius (30 AWG)	1.299			Inches
Bulk Cable Impedance	95	100	105	Ohms



III. Pin Assignments



Viewed from Top

Bottom Side Viewed from Bottom

IV. Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	3
9	LVTTL-I	ResetL	Module Reset	3
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3
12	LVCMOS- I/O	SDA	2-wire serial interface data	3
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3
18	CML-O	Rxln	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	3
28	LVTTL-O	IntL	Interrupt	3
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vccl	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	3
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Txlp	Transmitter Non-Inverted Data Input	3
37	CML-I	Txln	Transmitter Inverted Data Input	3
38		GND	Ground	1

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V. ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

VI. Mechanical Diagram



Revision History

Version No.	Date	Description
1.0	June 24, 2021	Preliminary datasheet

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